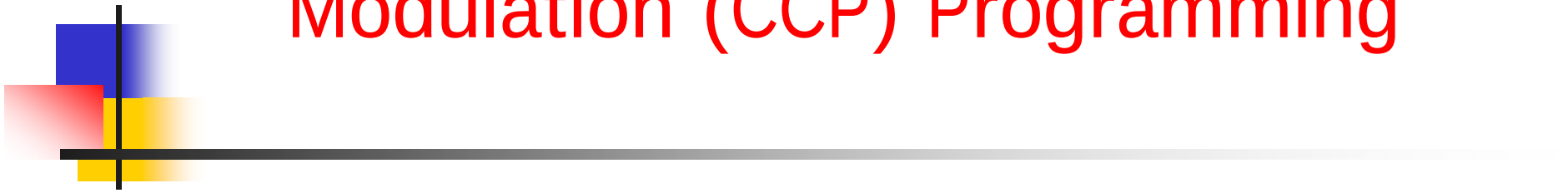
Capture/Compare/Pulse Width Modulation (CCP) Programming



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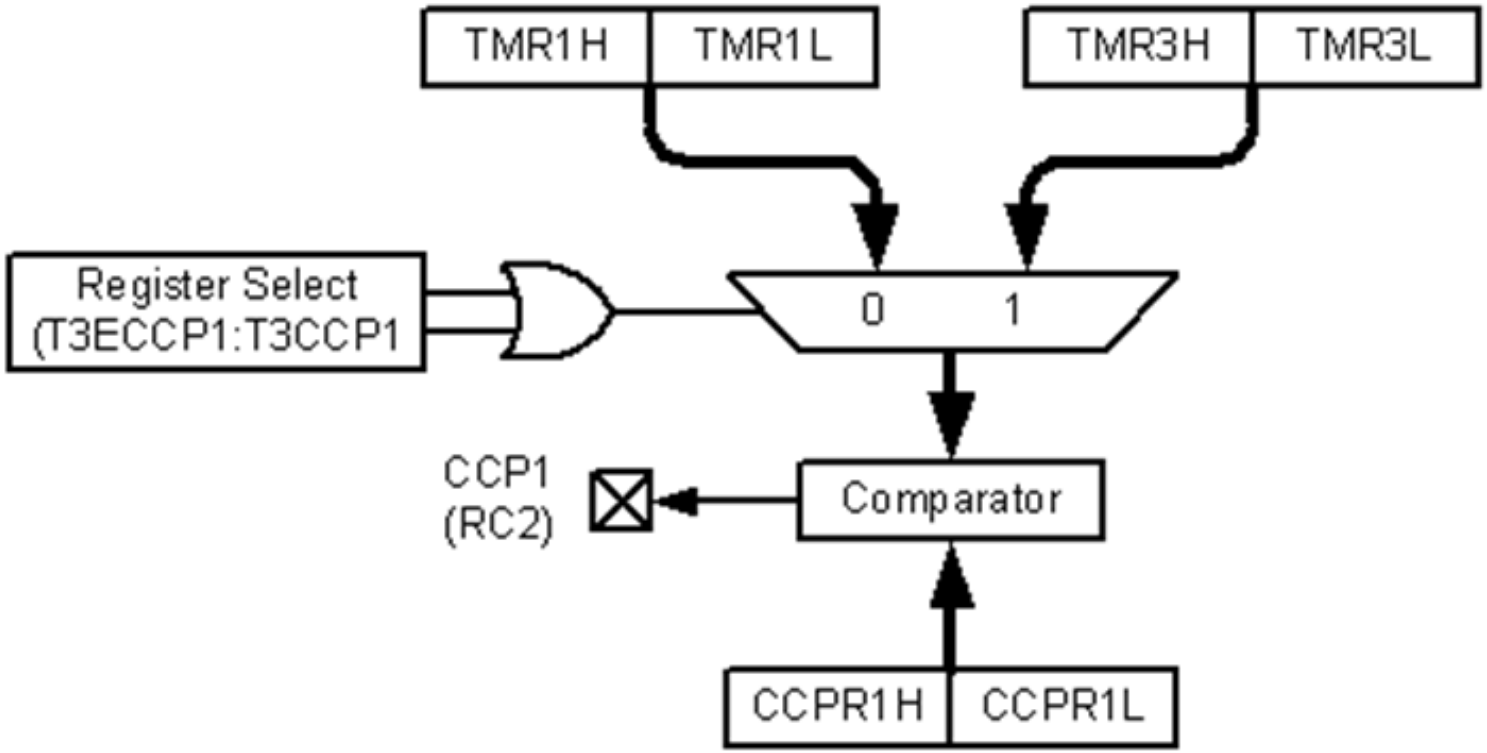
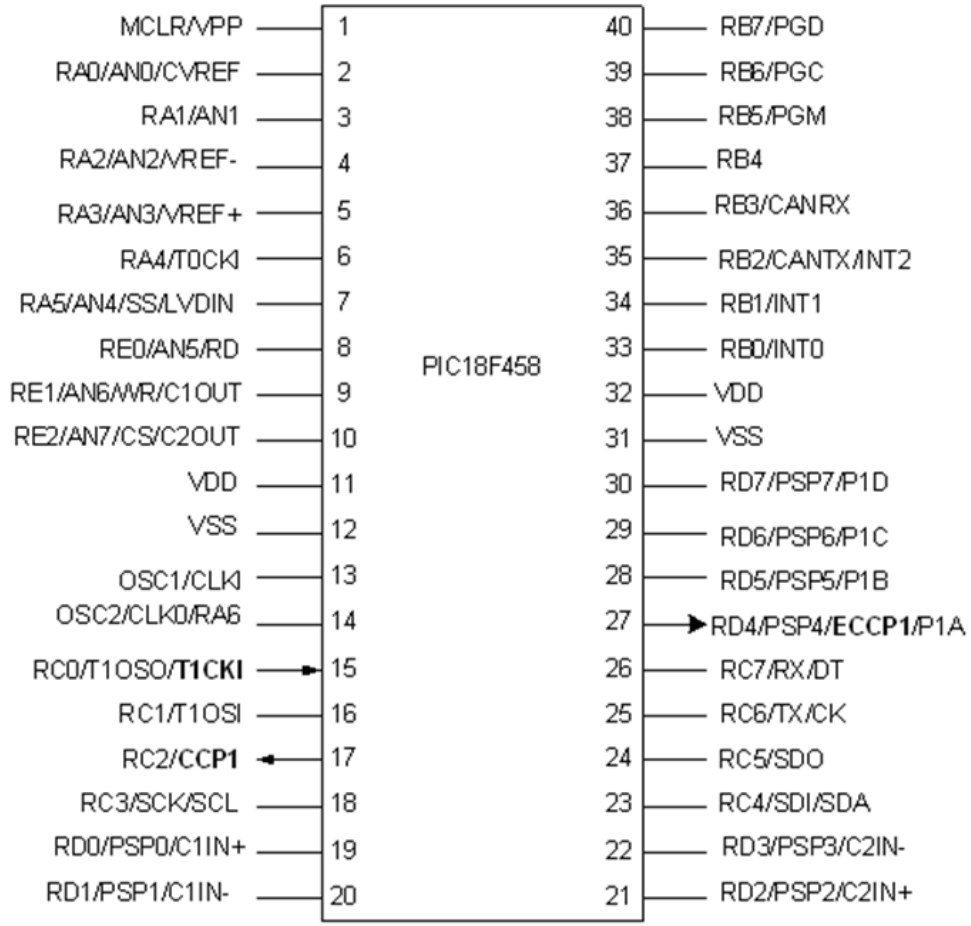
Compare mode



(Figure 15-6)

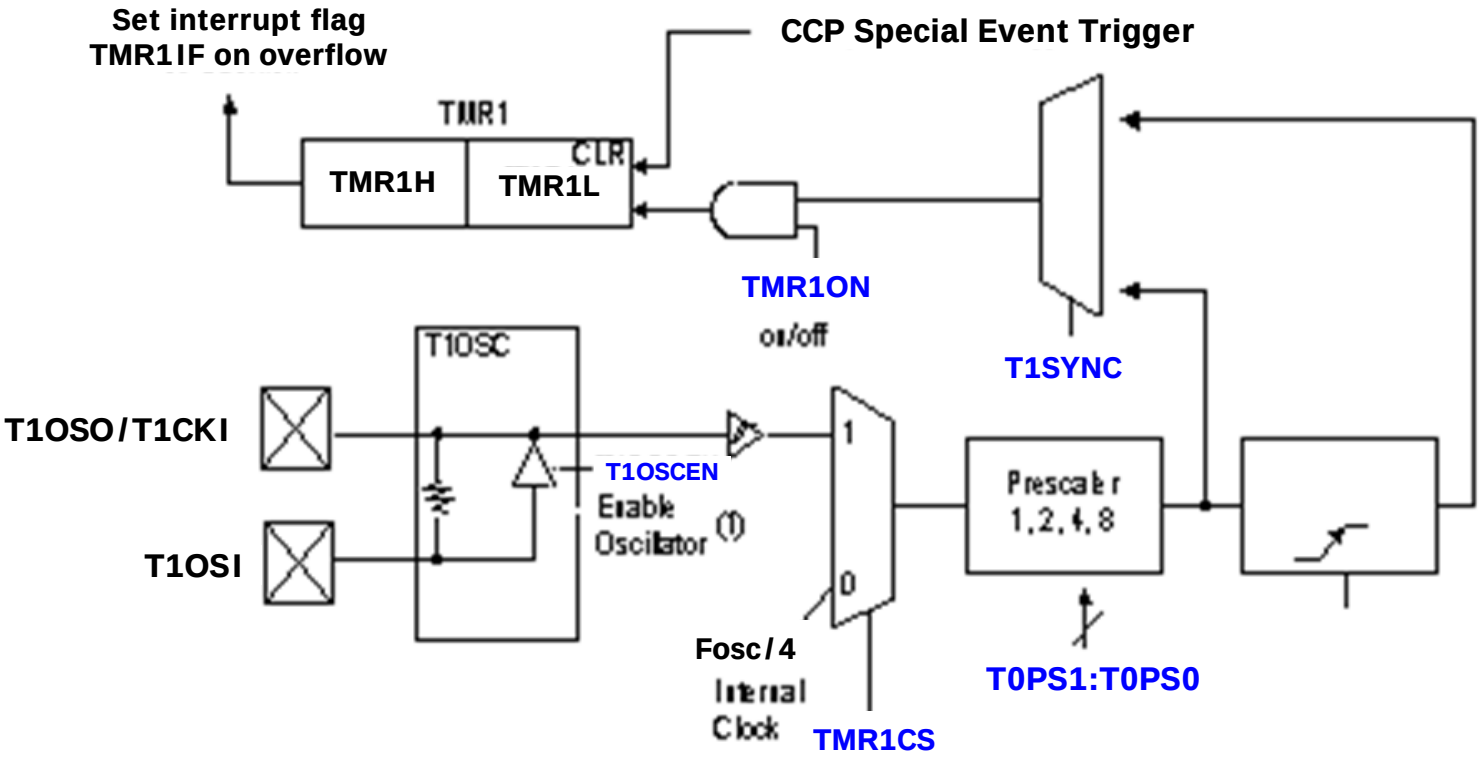
CCP high and low registers

CCP pins



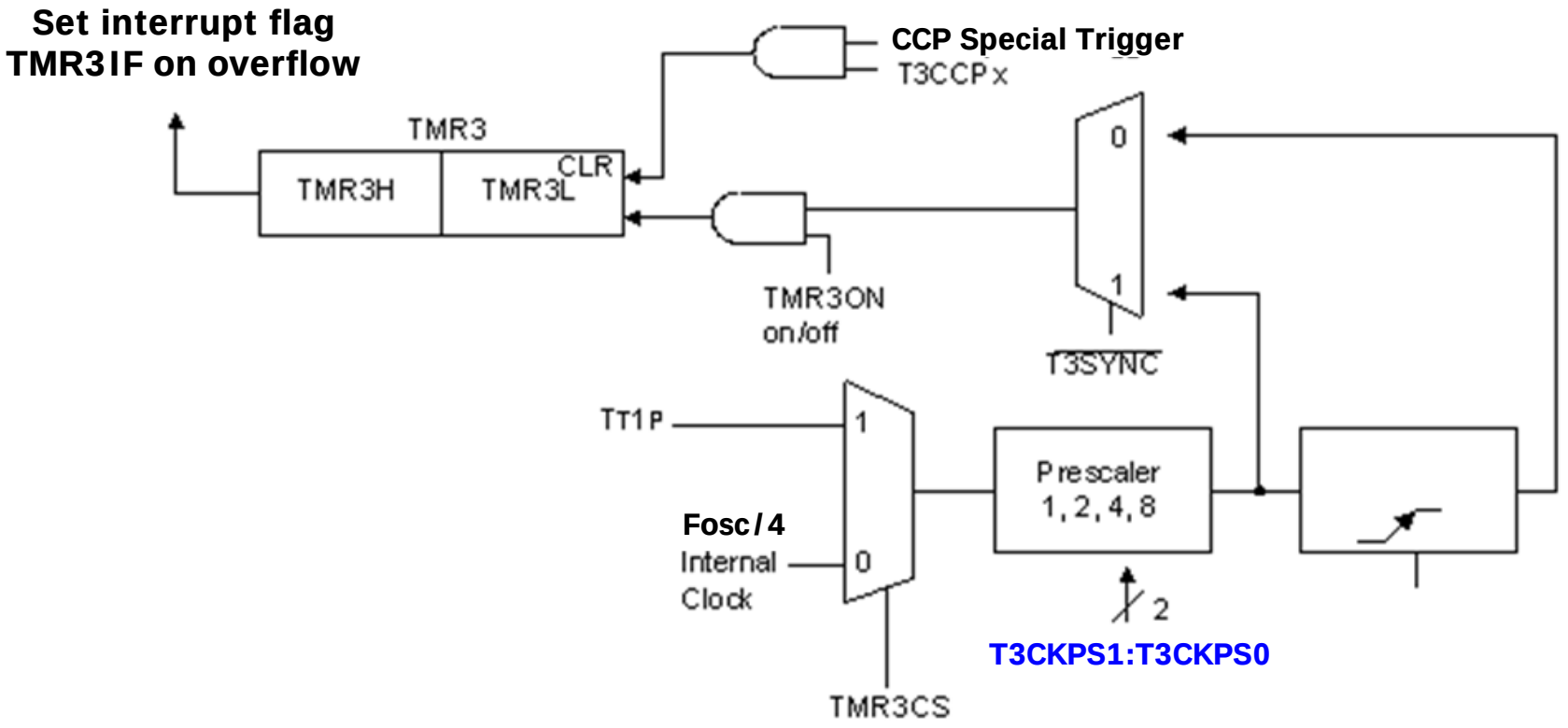
(Figure 15-3)

Timer1



(Figure 9-9)

Timer3 block diagram



(Figure 9-17)

Operation when a **match** occurs

- When the content of Timer1 (or Timer3) is equal to CCPR1H:CCPR1L.

  CCP1 pin perform one of the following actions

  - Toggle the CCP1 pin
  - Drive high the CCP1 pin
  - Drive low the CCP1 pin
  - Remain unaffected but generate software interrupt
  - Trigger a special event with a hardware interrupt and clear the timer

CCP1 control register

-	-	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0

DC1B1 Duty Cycle Bit 1. Used only in PWM mode.
Bit 1 of the 10-bit duty cycle register used in PWM

DC1B0 Duty Cycle Bit 0. Used only in PWM mode.
The least-significant bit (bit 0) of the 10-bit duty cycle register. Used in PWM.
The CCPxL register is used as bit 2 to bit 9 of the 10-bit duty cycle register.

(Figure 15-1)

CCP1 control register (cont.)

CCP1M3–CC1M0 CCP1 Mode Select

0 0 0 0	CCP1 is off
0 0 0 1	Reserved
0 0 1 0	Compare mode. Toggle CCP1 output pin on match. (CCP1IF bit is set.)
0 0 1 1	Reserved
0 1 0 0	Capture mode, every falling edge
0 1 0 1	Capture mode, every rising edge
0 1 1 0	Capture mode, every 4th rising edge
0 1 1 1	Capture mode, every 16th rising edge
1 0 0 0	Compare mode. Initialize CCP1 pin LOW, on compare match force CCP1 pin HIGH. (CCP1IF is set.)
1 0 0 1	Compare mode. Initialize CCP1 pin HIGH, on compare match force CCP1 pin LOW. (CCP1IF is set.)
1 0 1 0	Compare mode. Generate software interrupt on compare match. (CCP1IF bit is set, CCP1 pin is unaffected.)
1 0 1 1	Compare mode. Trigger special event. (CCP1IF bit is set, and Timer1 or Timer3 is reset to zero.)
1 1 x x	PWM mode

(Figure 15-1)

PIR1 (Peripheral interrupt flag register1)

CCP1IF CCP1IF Interrupt Flag bit

Compare Mode

0 = Timer1 (or Timer3) match did not occur.

1 = Timer1 (or Timer3) match occurred (must be cleared by software).

Capture Mode

0 = Timer1 (or Timer3) register capture did not occur.

1 = Timer1 (or Timer3) register capture occurred (must be cleared by software).

(Figure 15-5)

T3CON (Timer 3 control) register

RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON

RD16 D7 16-bit read/write enable bit
1 = Timer3 16-bit is accessible in one 16-bit operation.
0 = Timer3 16-bit is accessible in two 8-bit operations.

T3CCP2:T3CCP1 D6 D3 assigns Timer3 or Timer1 to CPP1 and CCP2 modules

	CCP1	ECCP1 (or CCP2)	
0 0 =	Timer1	Timer1	(clock source for compare/capture)
0 1 =	Timer1	Timer3	(clock source for compare/capture)
1 x =	Timer3	Timer3	(clock source for compare/capture)

T3CKPS1:T3CKPS0 D5 D4 Timer3 Input Clock Prescaler Selector

0 0 =	1:1	Prescale value
0 1 =	1:2	Prescale value
1 0 =	1:4	Prescale value
1 1 =	1:8	Prescale value

T1SYNC D2 Timer3 External Clock Input Synchronization Control bit
Used only when TMR3CS = 1 and clock comes from an external source. If TMR3CS = 0, this bit is not used.
1 = Do not synchronize external clock input.
0 = Synchronize external clock input.

TMR3CS D1 Timer 3 Clock Source Select bit
1 = External clock from pin RC0 (T1OSI or T1CKI)
0 = Internal clock (Fosc/4)

TMR3ON D0 Timer3 ON and OFF Control bit
1 = Enable (start) Timer3
0 = Stop Timer3

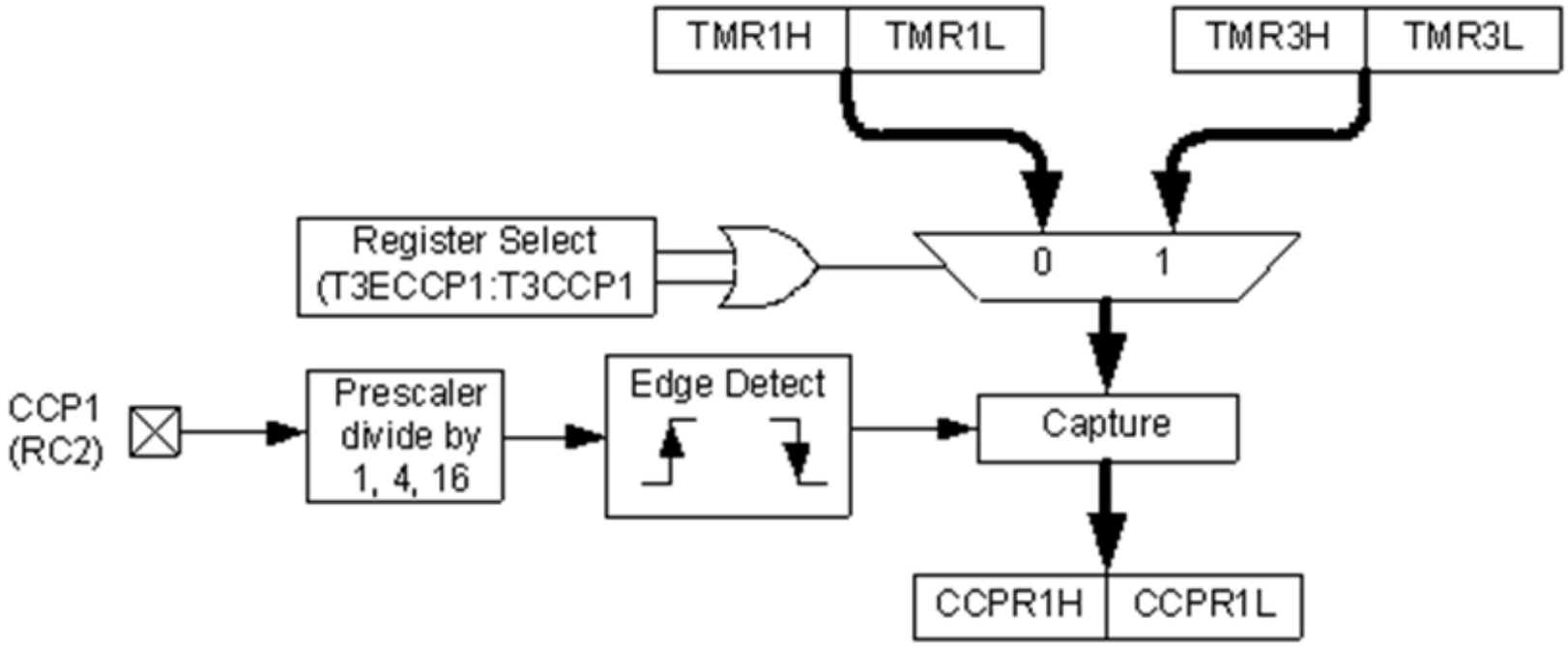
(Figure 15-4)

Compare mode programming

- Count external pulse, toggle LED every 10 pulses
  - Assembly (Program 15-1)
  - C (Program 15-1C)

- Generate a square wave with 50% duty cycle on CCP1 pin
  - Assembly (Program 15-2)
  - C (Program 15-2C)

Capture mode



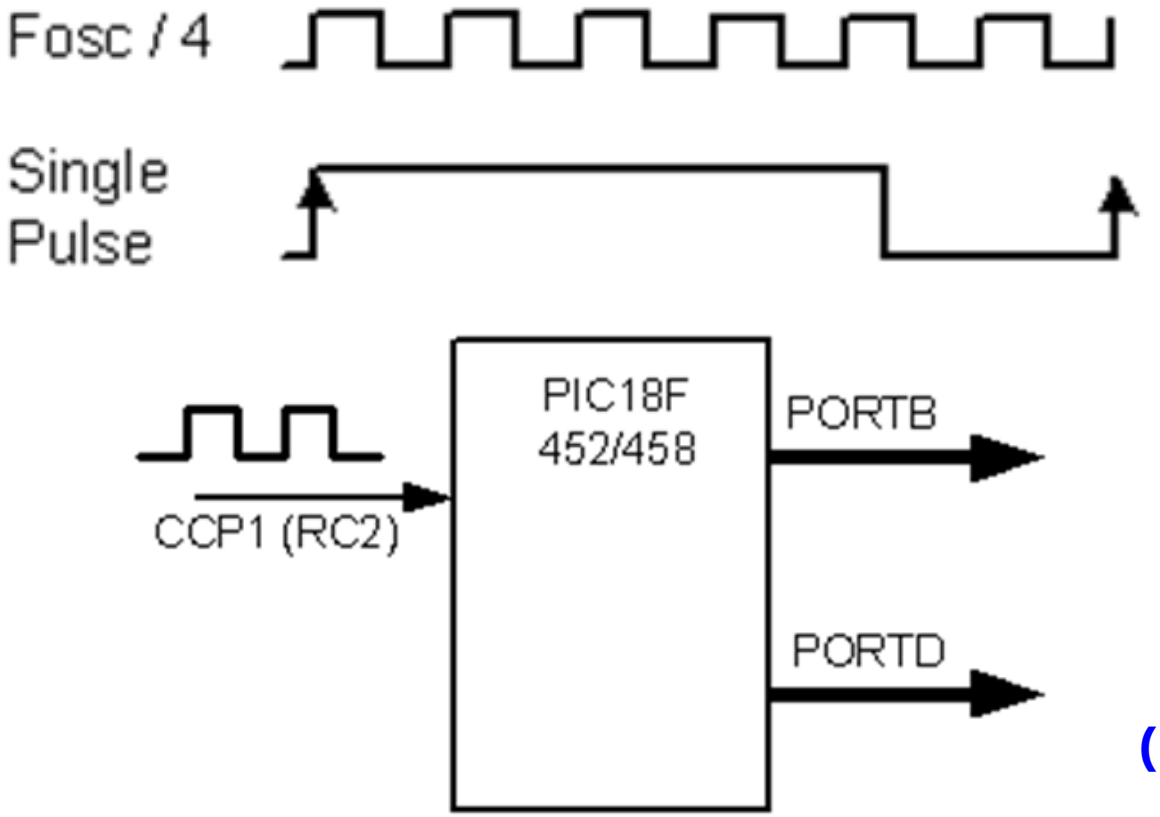
(Figure 15-9)

Capture mode operation

- An event at CCP pin cause the content of Timer1 (or Timer3) be loaded into CCPR1H:CCPR1L
  - every falling-edge pulse
  - every rising-edge pulse
  - every 4th rising-edge pulse
  - every 16th rising-edge pulse

Capture mode programming

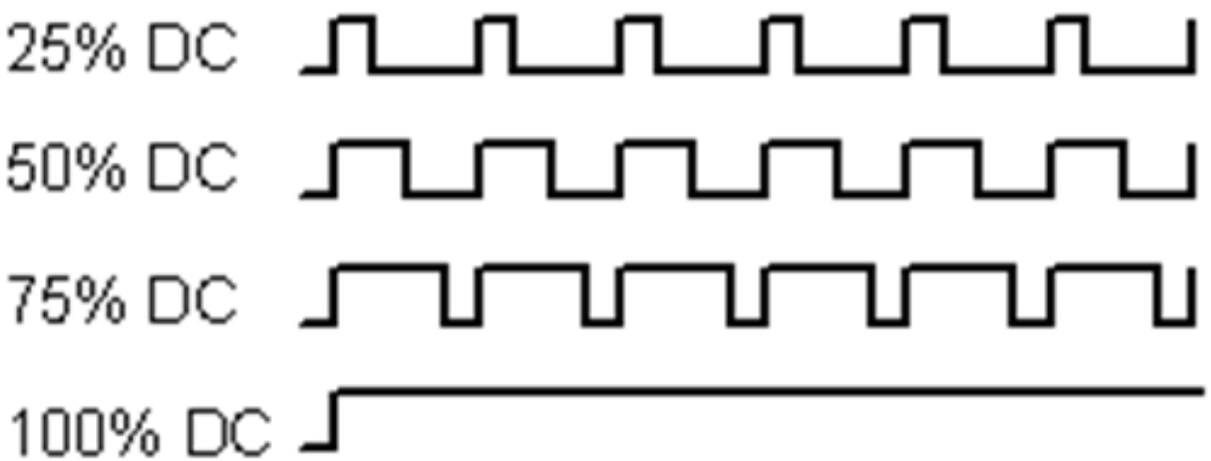
- Measure the period of a pulse using assembly (Program 15-3)
- Measure the period of a pulse using C (Program 15-3C)



(Figure 15-11)

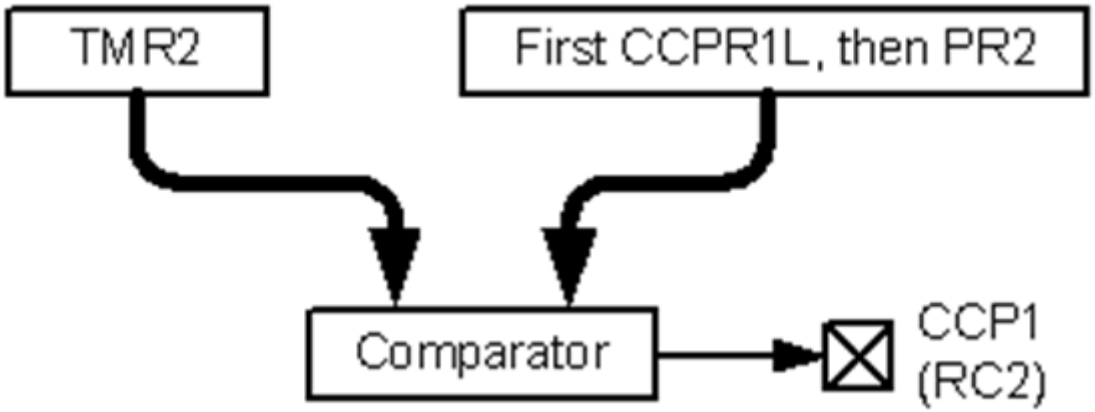
Pulse width modulation

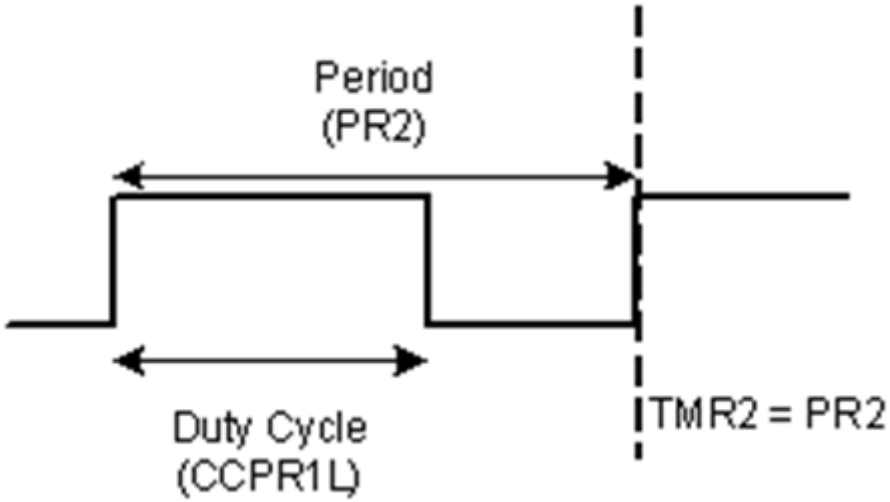
- Create pulses with variable widths
  - DC motor control



(Figure 15-13)

Pulse wide modulation (PWM) mode

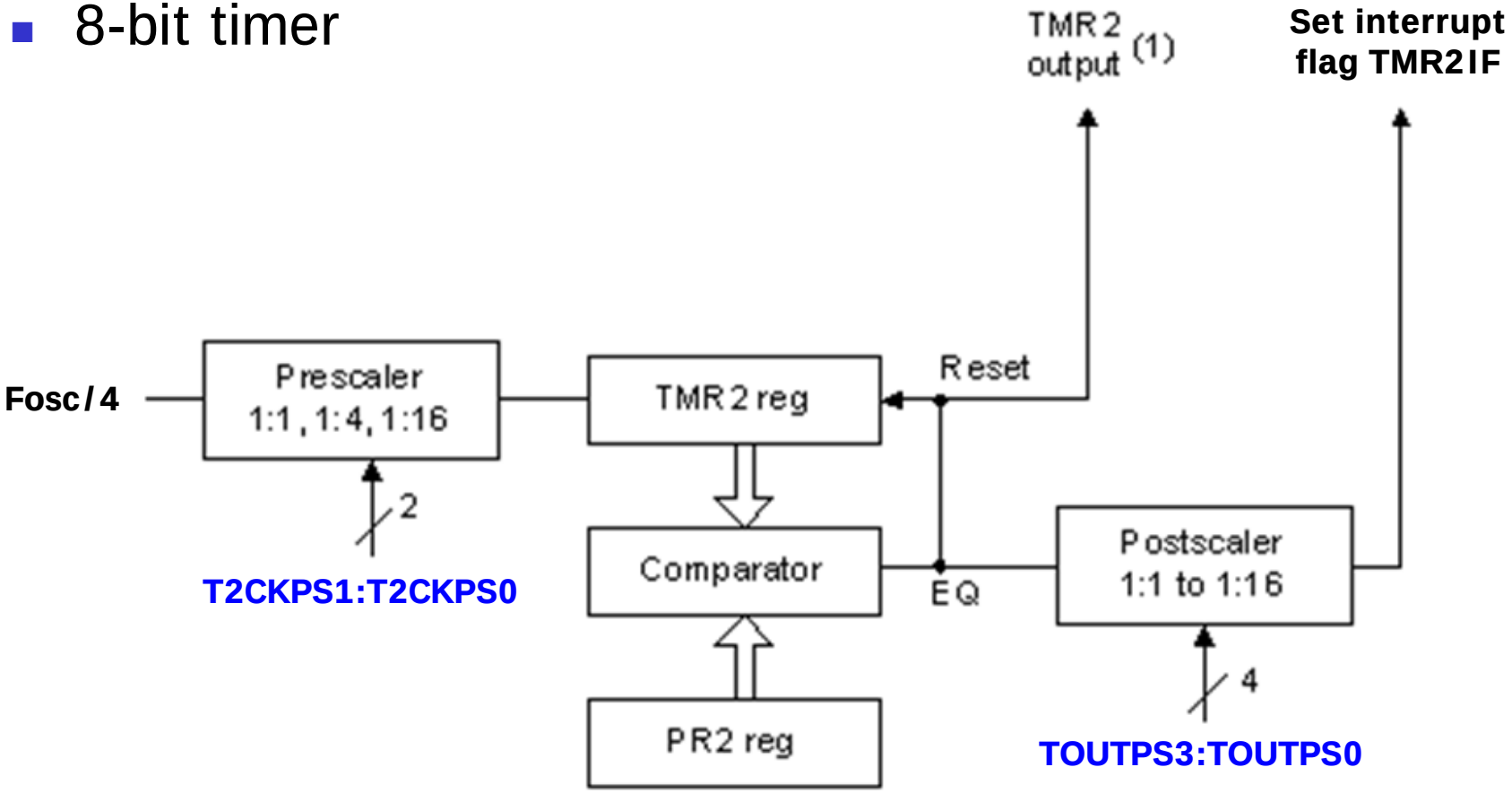




(Figure 15-17)

Timer2 block diagram

- 8-bit timer



(Figure 9-12)

CCP Special Event Trigger

Set the period and duty cycle of PWM

- Period of PWM
  - Tpwm = (PR2 + 1) x 4 x Tosc x N
    (N: prescaler of 1, 4, or 16)
- Duty cycle of PWM

DC1B1	DC1B0	Decimal points
0	0	0
0	1	0.25
1	0	0.5
1	1	0.75

Ex1. PR2 = 50 and 20% duty cycle ➔ 50*20%= 10

8-bit CCPR1L = 10 and 2-bit of DC1B1:0=00 00001010.00

Ex1. PR2 = 50 and 25% duty cycle ➔ 50*25%= 12.5

8-bit CCPR1L = 12 and 2-bit of DC1B1:0=10 00001100.10

PWM mode programming

- Generate a square wave with a 75% duty cycle (Program 15-5)
- Generate a square wave with a 75% duty cycle (Program 15-5C)

Reference

- M.A. Mazidi, R.D. Mckinlay, D Causey, PIC Microcontroller and Embedded Systems Using Assembly and C for PIC18, Pearson Education Inc., 2008.